IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DENNIS *et al.*
Application No.: 09/715,772
Filed: November 17, 2000
For: **Multi-Thread Peripheral Processing Using Dedicated Peripheral Bus**

Confirmation No.: 7033
Art Unit: 2111
Examiner: Justin King
Atty. Docket: 2222.4210001

Reply Brief Under 37 C.F.R. § 41.41

Mail Stop Appeal Brief - Patents

Commissioner for Patents
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Sir:

Appellants filed a Brief on Appeal to the Board of Patent Appeals and Interferences for the above-captioned application on May 18, 2006, appealing the decision of the Examiner in the Final Office Action mailed July 19, 2005. The Examiner's Answer was mailed on July 31, 2006. In reply to the Examiner's Answer, Appellants submit this Reply Brief Under 37 C.F.R. §41.41.

A. Rejection of claims 1-12, 14-25, 27-38, and 41 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,815,727 to Motomura

1. The Anticipation Rejection with Respect to Claims 1-7 and 10-12 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' independent claim 1. Appellants further disagree with the Examiner's interpretation of the present invention.

The Examiner indicates in the Response to Argument of the Examiner's Answer that "the alleged invention's processing slice executes several threads concurrently by

placing the plurality of threads on an execution pipeline; and by interleaving the threads, the processing slice alternatively processes the instruction from different threads while placing the earlier thread in a waiting state." Appellants believe this to be misdirected. Instead, claim 1 recites, in relevant part, "wherein the processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle." The processing slice accomplishes the concurrent execution of instructions in a clock cycle through the use of a thread control unit and one or more execution resources (*see, e.g.*, FIG. 4, Element 470; FIG. 4, Elements 420, 430, 440, 450, and 460).

Unlike Motomura, in an embodiment of the claimed invention, the earlier thread does not generally enter a waiting state. The execution of a "wait" or "no_wait" instruction by a thread in a processing slice is relevant only to a peripheral operation. (Specification, p. 9, ll. 13-15; p. 11, ll. 6-16). During the execution of a peripheral operation (even a "wait" operation), instructions may be dispatched and processed concurrently, on a common clock cycle, from several threads to the register file 430, the condition code memory 440, the functional unit 450, or the memory access unit 460. (Specification, p. 10, ll. 21-25). Accordingly, it is proper to say that the "processing slice executes the instructions from more than one of the plurality of threads concurrently in a clock cycle," as recited in independent claim 1.

Motomura, on the other hand, does not execute the instructions from more than one thread concurrently in a clock cycle. On the contrary, each processor in Motomura can execute only one thread at a time, and it is disclosed that each thread must go into a "waiting" or "completed" state before another thread is assigned to the processor. (Motomura, col. 8, ll. 40-51).

The Examiner further argues that "as stated in the rejection, it is the transaction requestor as the peripheral units, not the multithread executing system as alleged by the appellant been matched to the peripheral unit." Applicants submit that the transaction requestor and the multithread executing system of Motomura are one and the same. Motomura states that "when the processor 110 forks other threads during execution of a certain thread, a fork demand is transferred to the ordered multithread executing system 120 via the demand transfer line 112." (Motomura, col. 8, ll. 18-21). It furthermore constitutes the I/O component described by the Examiner (Examiner's Answer, p. 16) capable of submitting requests to Motomura's processor (Motomura, col. 8, ll. 27-39). Accordingly, the Appellants submit that the Examiner's characterization of Motomura's parallel processing system 100 as equivalent to the processing slice of Appellants' specification is incorrect. The parallel processing system 100 in Motomura does not interface with a peripheral unit over a peripheral bus as required by independent claim 1. Neither can the multithread executing system 120 in Motomura be characterized as a peripheral unit of parallel processing system 100 since it is located entirely within the parallel processing system 100.

The Examiner adds that "other prior arts on record ... also evidences that both the processor and I/O devices are known components in a computer system." (Examiner's Answer, p. 16). This statement, coupled with the inability of the I/O component in Motomura to serve as the comparable peripheral unit as reflected in independent claim 1, does not present proper grounds for rejection under 35 U.S.C. § 102(b), as the combination of other teachings to remedy the deficiencies of Motomura has not been presented as a proper rejection to which the Appellants can reasonably respond.

Since Motomura does not teach or suggest each and every feature of independent claim 1 it does not anticipate that claim. Accordingly, the Examiner's rejection of claim 1 must be reversed. Furthermore, dependent claims 2-7 and 10-12 are also not anticipated by Motomura for at least the same reasons as independent claim 1 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 2-7 and 10-12 must also be reversed.

2. The Anticipation Rejection with Respect to Claims 14-20 and 23-25 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 14-20 and 23-25. Appellants submit that claims 14-20 and 23-25 are distinguishable over Motomura for the additional reasons provided with respect to independent claim 1 in this Reply Brief.

3. The Anticipation Rejection with Respect to Claims 27-33 and 36-38 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 27-33 and 36-38. Appellants submit that claims 27-33 and 36-38 are distinguishable over Motomura for the additional reasons provided with respect to independent claim 1 in this Reply Brief.

4. The Anticipation Rejection with Respect to Claim 41 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claim 41. Appellants submit that claim 41 is distinguishable over Motomura for the additional reasons provided with respect to independent claim 1 in this Reply Brief.

5. *The Anticipation Rejection with Respect to Claims 8 and 9 is in Error and Must be Reversed*

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 8 and 9. Appellants submit that claims 8 and 9 are distinguishable over Motomura for the additional reasons provided with respect to independent claim 1, from which they depend, in this Reply Brief.

Furthermore, the Examiner incorrectly describes the Appellants' argument in the Appellants' Appeal Brief by characterizing it as "Appellant's argument that Motomura does not disclose the waiting instruction." (Examiner's Answer, p. 16). On the contrary, Appellants' acknowledge that Motomura may disclose a waiting state, but disagree at the very least on the entry into the aforementioned waiting state conditioned on a "command message" as disclosed in claims 8 and 9. Additionally, operations transmitted to Motomura's equivalent to the "peripheral unit" do not come in "wait" and "non-wait" variants.

Accordingly, since Motomura does not teach or suggest each and every feature of claims 8 and 9 it does not anticipate those claims, and the Examiner's rejection of claims 8 and 9 must be reversed.

6. *The Anticipation Rejection with Respect to Claims 21 and 22 is in Error and Must be Reversed*

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 21 and 22. Appellants submit that claims 21 and 22 are distinguishable over Motomura for the additional reasons provided with respect to claims 8 and 9 in this Reply Brief.

7. The Anticipation Rejection with Respect to Claims 34 and 35 is in Error and Must be Reversed

Appellants maintain their position that Motomura does not teach or suggest each feature of Appellants' claims 34 and 35. Appellants submit that claims 34 and 35 are distinguishable over Motomura for the additional reasons provided with respect to claims 8 and 9 in this Reply Brief.

B. Rejection of claims 13, 26, and 39 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,418,917 to Hiraoka et al.

Appellants maintain their position that the combination of Motomura and Hiraoka does not teach or suggest each feature of Appellants' claims 13, 26, and 39.

C. Rejection of claim 40 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,815,727 to Motomura in view of U.S. Patent No. 5,938,765 to Dove et al.

Appellants maintain their position that the combination of Motomura and Dove does not teach or suggest each feature of Appellants' claim 40.

D. Conclusion

In light of the arguments above, as well as those set forth in Appellants' Brief on Appeal filed May 18, 2006, Appellants respectfully submit that the final rejections of claims 1-41 are improper and should be reversed.

Respectfully submitted,

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